Hi3520D H.264 Codec Processor

Brief Data Sheet

Issue 02

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Hi3520D H.264 Codec Processor

Key Specifications

Processor Core

ARM Cortex A9 @ max. 660 MHz
- 32 KB L1 I-cache and 32 KB L1 D-cache
- 128 KB L2 cache

Video Encoding and Decoding

H.264 Baseline/Main/High Profile Level 4.2
MJPEG/JPEG baseline encoding/decoding

Video Encoding and Decoding

H.264&JPEG multi-stream encoding and decoding:
- 8xD1@6 fps+8xCIF@6 fps encoding+8xD1@6 fps decoding+JPEG snapshot D1@16 fps
- 8xCIF@30 fps +8xQCIF@30 fps encoding+8xCIF@30 fps decoding +JPEG snapshot D1@16 fps
- 4xD1@30 fps+4xCIF@30 fps encoding+4xD1@30 fps decoding+ JPEG snapshot D1@8 fps
- 4x960H@30 fps+4xCIF@30 fps encoding+1x960H@30 fps decoding+ JPEG snapshot 960H@8 fps
- 8xD1@30 fps H.264 decoding
- 4x720p@30 fps H.264 decoding

CBR or VBR ranging from 16 kbit/s to 40 Mbit/s
Encoding frame rate ranging from 1 fps to 60 fps
ROI encoding
Generating and encoding grayscale video from color video

Intelligent Video Analysis

Integrated intelligent analysis acceleration engine, supporting motion detection, boundary security, and video diagnosis

Video and Graphic Processing

Video pre- and post-processing, including de-interlacing, image enhancement, edge enhancement, and 3D denoising
Anti-flicker processing on output videos and graphics
1/8x to 16x video scaling
1/2x to 2x graphic scaling
Up to eight OSDs for video before encoding
Alpha blending of video layers and graphics layers for video displaying

Audio Encoding and Decoding

Hard-wired audio encoder, supporting ADPCM, G.711, and G.726 encoding
Software encoding and decoding complying with various standards

Security Engine

AES, DES, and 3DES encryption and decryption

Video Interfaces

Video input interfaces
- 2xBT.656@108 MHz/144 MHz for 8xCIF/8xD1/8x960H real-time inputs
- 2xBT.656@148.5 MHz for 2x720P real-time inputs
- 1xBT.1120@148.5 MHz for 1x1080p real-time inputs

Video output interfaces
- HDMI 1.3+VGA+CVBSx2 outputs. The HDMI and VGA outputs share the same source
- Maximum resolution 1080p@60 fps for HDMI or VGA
- Three graphics layers in RGB1555 or RGB8888 format, with the maximum resolution of 1920x1080
- One hardware cursor layer in RGB1555 or RGB8888 format, with the maximum resolution of 128x128
- CVBS0 video layer can be used as the HD PIP layer

Audio Interfaces

Two I^2S interfaces
- One input interface
- One output interface

Ethernet Port

One Ethernet port
- Integrated FE PHY
- MDI at the PHY layer or RMII at the MAC layer
- 10/100 Mbit/s
- full-duplex or half-duplex mode

Integrated FE PHY

Peripheral Interfaces

Two SATA 2.5 interfaces
- PM
- eSATA

Four UART interfaces
One SPI, supporting two CSs
One IR interface, one I^2C interface, and multiple GPIO interfaces
Two USB 2.0 host ports, supporting hub

Memory Interfaces

One 16-bit DDR2/DDR3 SDRAM controller interface
- Maximum frequency of 660 MHz
- ODT
- Maximum capacity of 512 MB
- Automatic power consumption control

SPI NOR flash interfaces
- 1-, 2-, or 4-bit SPI NOR flash interfaces
- Two CSs
- Maximum capacity of 32 MB for each CS

Built-in 4 KB BOOTROM and 10 KB SRAM

RTC with Separated Power Supply

Independent power supply for the RTC by using batteries
Built-in temperature sensor
Automatic correction of RTC counting frequency based on the temperature

Boot Modes

Boots from the BOOTROM.
Boots from the SPI NOR flash.

SDK

Linux 3.0-based SDK

High-performance H.264 decoding PC library

Physical Specifications

Power consumption

- 2.5 W typical power consumption
- Multi-level power-saving control

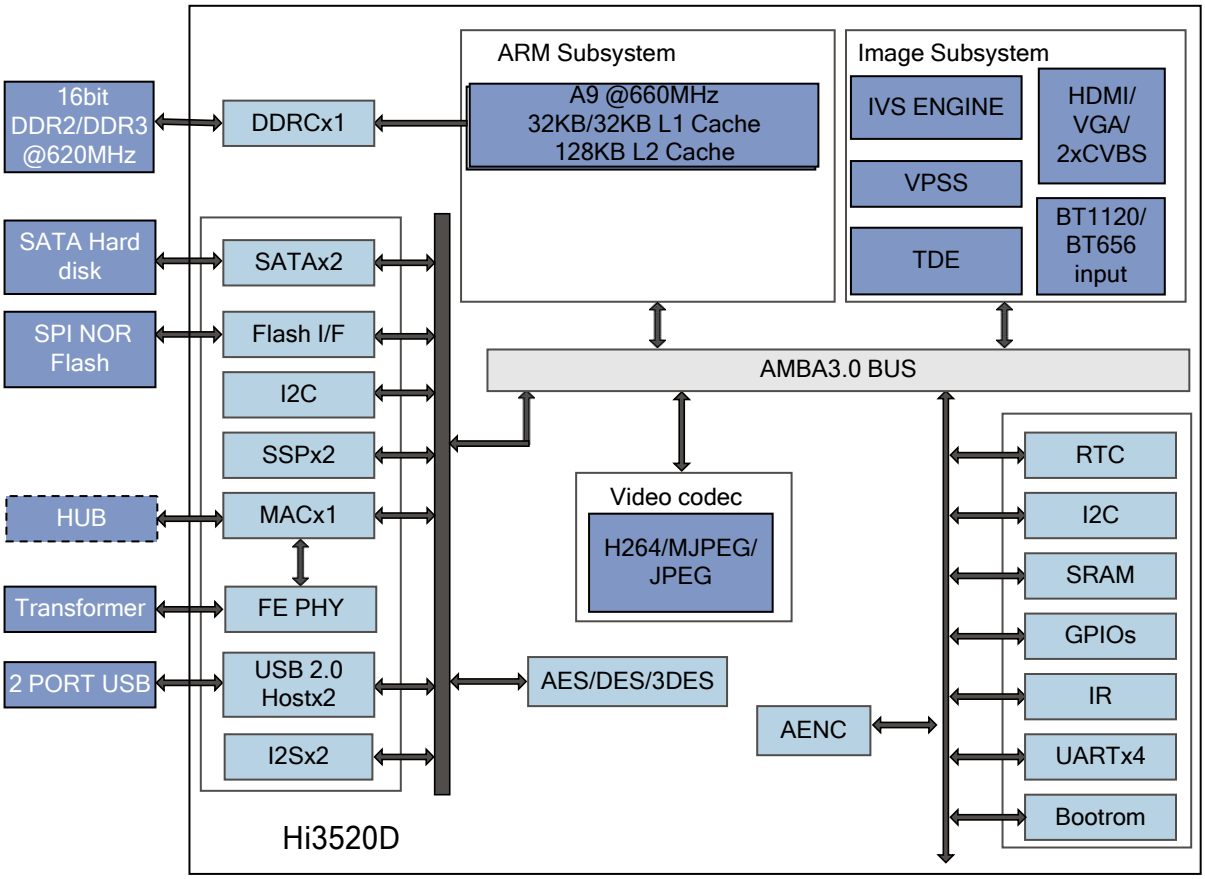
Operating voltage

- 1.25 V core voltage
- 3.3 V I/O voltage
- 1.5 V or 1.8 V DDR2/DDR3 SDRAM interface voltage

Package

- RoHS, Epad-LQFP256
- Ball pitch: 0.4 mm (0.016 in.)
- Body size: 28 mm x 28 mm (1.1 in. x 1.1 in.)

Functional Block Diagram



The Hi3520D is a professional SoC designed for multi-channel D1, HD DVRs, and HD NVRs. With a high-performance A9 processor and an engine supporting up to 8-channel D1 encoding and decoding, the Hi3520D meets the rising demand for HD applications. The Hi3520D also integrates an outstanding video processing engine, various encoding/decoding algorithms, and multi-channel HD output capability. These features provide users with high-quality image experience. In addition, the Hi3520D integrates various peripheral interfaces to meet customer requirements for functionality, features, and image quality, while reducing the EBOM cost.

DVRs (Each with a Hi3520D)

4xD1 DVR

4xD1+4xCIF dual-stream real-time encoding+JPEG snapshot D1@8 fps +4xD1 real-time decoding
HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs

4x960H DVR

4x960H+4xCIF encoding+1x960H real-time decoding
HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs

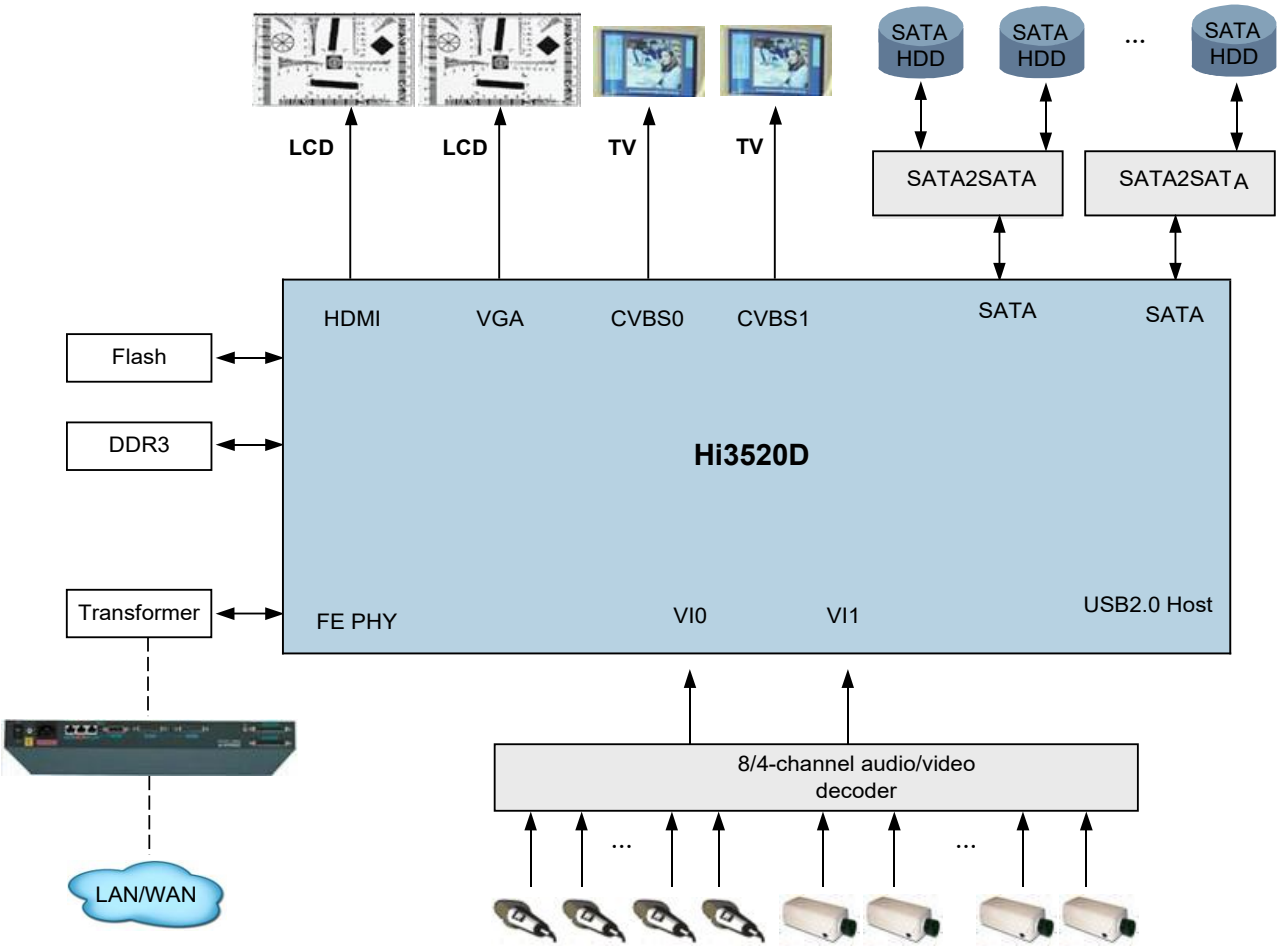
8xCIF DVR

8xCIF+8xQCIF encoding+JPEG snapshot D1@16 fps +8xCIF real-time decoding

HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs

8xD1 DVR

8xD1@6fps+8xCIF@6fps dual-stream encoding +1xD1@6fps decoding
HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs



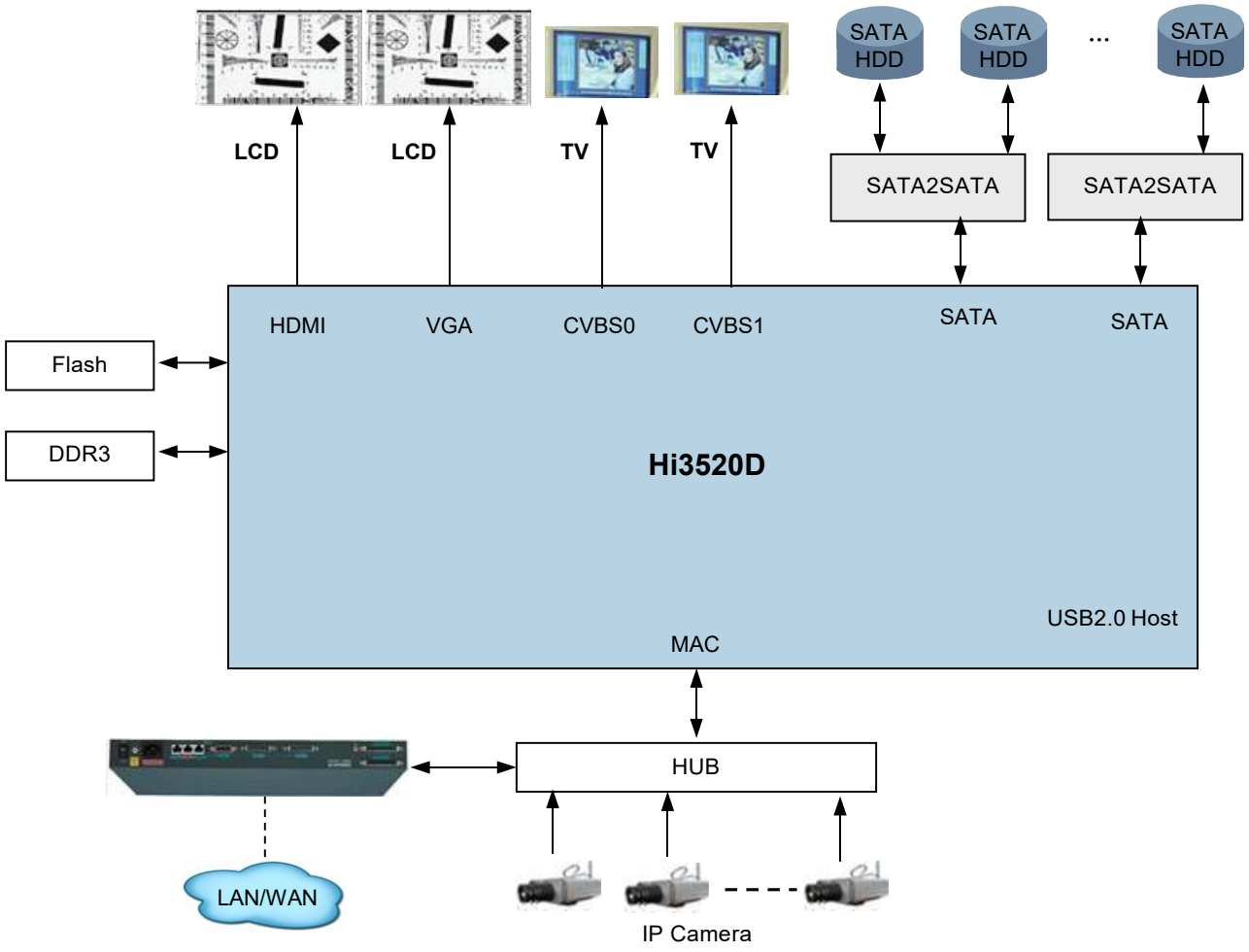
NVRs (Each with a Hi3520D)

8xD1 NVR

8xD1 real-time decoding
HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs

4x720p NVR

4x720 real-time decoding
HDMI+VGA 1080p@60 fps outputs from the same source+2-channel CVBS outputs



Acronyms and Abbreviations

ABR	available bit rate
CBR	constant bit rate
CS	chip select
GPIO	General Purpose Input/Output
LAN	local area network
MAC	Media Access Control
MJPEG	Motion Joint Photographic Experts Group
RoHS	restriction of the use of certain hazardous substances
VBR	variable bit rate
VPSS	video process subsystem
WAN	wide area network